Yadanabon University Research Journal, 2019, Vol-10, No.1

Design and Implementation of FPGA-Based 3-Digit 7-Segments LED Display Counter

Yi Yi Swe*

Abstract

The FPGA-based 3-digit 7-segments LED display counter is designed and constructed by using Altera's Cyclone FPGA, 3-digit 7-segments LED display and other supported electronic components. The core FPGA board based on Cyclone IV FPGA is used as the main control unit. The FPGA board is programmed by using VHDL (Very high speed integrated circuit Hardware Description Language) language. The peripheral circuits (such as switch input circuit, LED display circuit, 7-segments LED display) are also constructed to test the function of the FPGA and VHDL language. Finally, the constructed display counter is tested by writing various programs and downloading the file into the FPGA board. The constructed board can count numbers "000" up to "999". It can be used in various fields such as count up, count down, stop watch and other counting applications.

Key words: FPGA, LED display, counter, VHDL

Introduction

In digital logic and computing, a counter is a device which stores (and sometimes displays) the number of times a particular event or process has occurred, often in relationship to a clock signal. The most common type is a sequential digital logic circuit with an input line called the clock and multiple output lines. The values on the output lines represent a number in the binary or BCD number system. Each pulse applied to the clock input increments or decrements the number in the counter.

A counter circuit is usually constructed of a number of flip-flops connected in cascade. Counters are a very widely used component in digital circuits, and are manufactured as separate integrated circuits and also incorporated as parts of larger integrated circuits.

The logic devices are basic building blocks of the digital circuits. The logic devices can be classified into two broad categories - fixed and programmable logic devices. The circuits in a fixed logic device such as 7400- or 4000- series ICs are permanent, they perform one function or set of functions - once manufactured, they cannot be changed. With fixed logic devices, the time required to go from design, to prototypes, to a final manufacturing run can take from several months to more than a year, depending on the complexity of the device. And, if the device does not work properly, or if the requirements change, a new design must be developed.

On the other hand, programmable logic devices (PLDs) are standard, off-the-shelf parts that offer customers a wide range of logic capacity, features, speed, and voltage characteristics - and these devices can be changed at any time to perform any number of functions. With programmable logic devices, designers use inexpensive software tools to quickly develop, simulate, and test their designs. Then, a design can be quickly programmed into a device, and immediately tested in a live circuit. Hundreds, or even thousands, of digital logic ICs will be replaced by a single PLD.

Basically, there are four types of PLDs: simple programmable logic devices (SPLDs), complex programmable logic devices (CPLDs), field-programmable gate arrays (FPGAs), and application-specific integrated circuits (ASICs). The FPGA board will be designed and constructed in this research work to do digital electronics experiments in the place of 7400- and 4000- series logic devices. The functional block diagram of the constructed FPGA-based 3-digit 7-segments LED display counter is shown in figure 1.

* Lecturer, Dr., Department of Physics, Yadanabon University

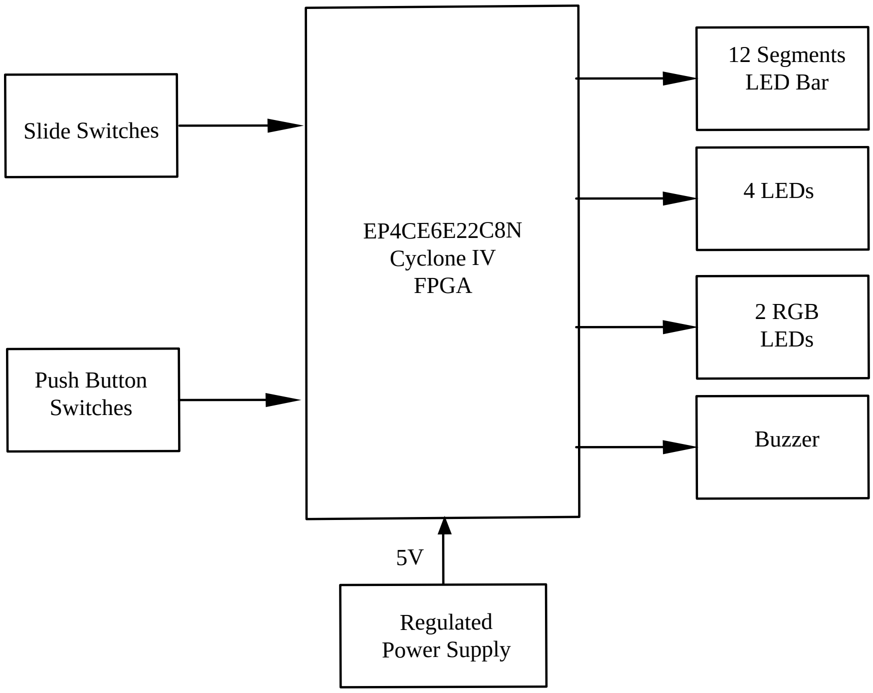


Fig.1 The functional block diagram of the constructed FPGA-based 3-digit 7-segments LED display counter

Electronic Devices Used in this Research Work

The design and construction of FPGA-based 3-digit 7-segments LED display counter will be explained in this section. Firstly the features and functions of the Altera's Cyclone IV FPGA board used in this research work will be described. The constructed input switch circuits, LED display circuits and buzzer circuit will be described. Finally, the hardware description language implementation required for the counter circuit design will be discussed.

The EP4CE6 Cyclone IV FPGA Core Board

A Field-Programmable Gate Array (FPGA) is an array of gates interconnected in a row-column matrix that can be programmed in the field by a computer via a USB connection. The FPGA differs from the CPLD in that, instead of solving the logic design by interconnecting logic gates, it uses a look-up table (LUT) method to resolve the particular logic requirement. This allows PLD manufacturers to form a more streamlined design, creating a much denser and faster PLD. Besides having thousands of internal logic elements, FPGAs have hundreds of I/O pins with programmable internal interconnects and storage registers.

The EP4CE6 is an FPGA core board from Waveshare, China, based on the Altera's Cyclone IV EP4CE6E22C8N device. The core board has the features: onboard Serial Configuration Device EPCS16SI8N, integrated FPGA basic circuit, such as clock circuit, onboard nCONFIG button, RESET button, 4 x LEDs, all the I/O ports are accessible on the pin headers, onboard JTAG debugging/programming interface and 2.54 mm header pitch design, suitable for being plugged-in application system.

The EP4CE6E22C8N, the Altera's Cyclone IV FPGA device has the features: **o**perating frequency of 50MHz, **o**perating voltage range of 1.15V～3.465V, QFP144 package, 80 I/O pins, 6K of logical elements (LEs), 270kb RAM, 2 PLLs and supports JTAG Debugging/Programming. The CoreEP4CE FPGA core board is shown in figure 2.

Fig.2 The FPGA core board.

The FPGA Base Board

The constructed FPGA base board mainly consists of input switch circuits, LED display circuits, three digits 7-segments display circuit and buzzer circuit. The photograph of the constructed FPGA base board is shown in figure 3.


Fig.3 Constructed FPGA base board.

Input Switch Circuits

The input switch circuits are shown in figure 4. There are two switch circuits: slide switch circuit and push button switch circuit. The slide switch circuit consists of 12 three terminals slide switches. One terminal of switch is connected to 3.3 V power output from the FPGA core board. The other end is connected to ground. The middle one (output terminal) is used as the switch output and connected with the FPGA pins. The circuit can be used to produce digital logic outputs (“0” or “1”). Twelve digital data inputs can be obtained by using the circuit. The connected FPGA pins are also shown in the figure. The push button switch circuit consists of 4 push button switches. One terminal of the switch is connected to 3.3 V supply from the FPGA board through the current limiting resistor. Other terminal of the switch is grounded. Four switch outputs are obtained by taken outputs between switch terminals and current limiting resistors. The outputs of the push button circuits are normally “HIGH” outputs. The outputs are connected to the FPGA pins. The assigned FPGA pins are shown in figure 4.

LED Display Circuits

The LED display circuits used in this research work mainly consists of 12 segments LED bar circuit, 4 LEDs circuit, 2 RGB LEDs circuit and 3 digits 7-segment LED display circuit. The 12 segments LED bar circuit is shown in Fig. 4. Is consists of 12 LEDs arranged as LED bar. The current limiting resistors (490 Ω) are connected in series with the anodes of the LEDs. Other ends of the resistors are used to accept data from FPGA output pin. The cathodes of the LEDs are grounded. Similarly 4 LEDs circuit and 2 RGB LEDs circuit are constructed. The 3 digits 7-segment LED display circuit is the common anode multiplexing type. There are 11 input pins (8 for segments and 3 for digit select). The segments a, b, c, d, e, f, g and decimal point (dp) as well as digit select pins (1, 2 and 3) are connected to the FPGA pins via current limiting resistors. The FPGA pins for the LED display circuits are also shown in figure 4.

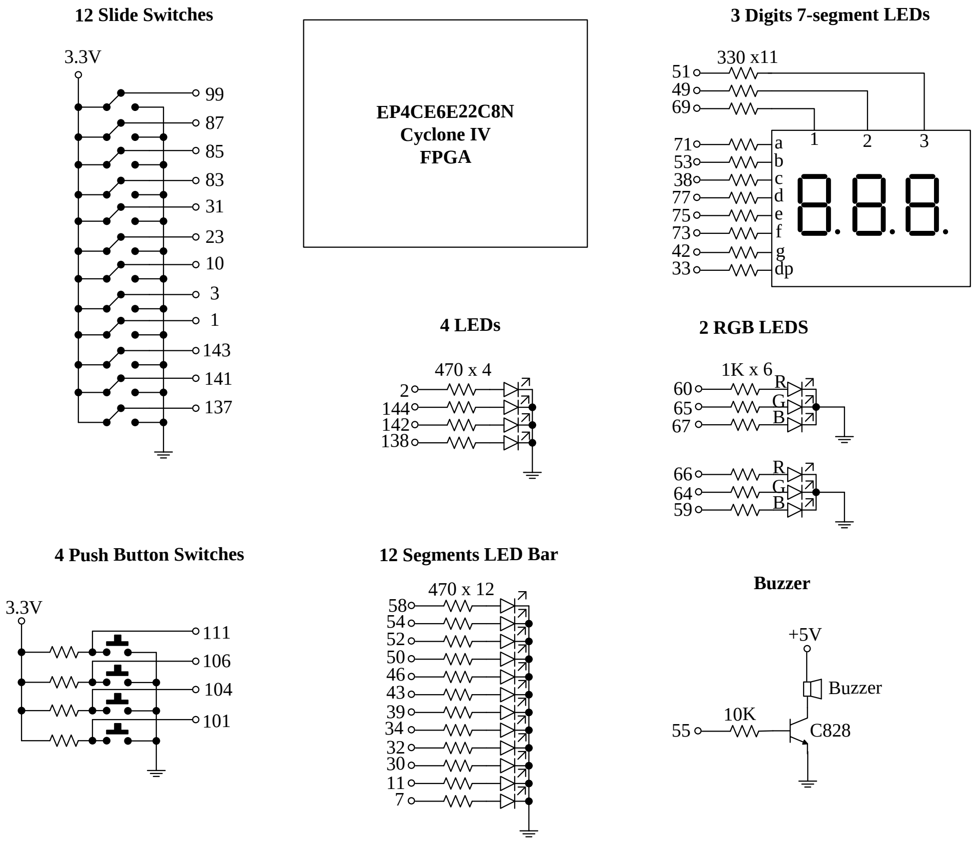


Fig.4 The complete circuit diagram

Implementation of VHDL Hardware Description Language

Hardware description language (HDL) design is based on the creation and use of textural based descriptions of a digital logic circuit or system. By using a particular HDL (the two IEEE standards in common use in industry and academia are Verilog-HDL and VHDL, the description of the circuit can be created at different levels of abstraction from the basic logic gate description according to the language syntax (the grammatical arrangement of the words and symbols used in the language) and semantics (the meaning of the words and symbols used in the language).

In VHDL (Very high speed integrated circuit Hardware Description Language), a design is created initially as an entity declaration and an architecture body. The entity declaration describes the design I/O and includes parameters that customize the entity. The entity can be thought of as a black box with visible I/O connections. The architecture body describes the internal working of the entity and contains any combination of structural, dataflow, or behavioral descriptions used to describe the internal working of the entity.

In this research, the Altera's Quartus (Quartus Prime 17.0) lite software is used to implement 3-digit 7-segment LED display counter circuit in VHDL hardware description language. The Quartus Prime system includes full support for all of the popular methods of entering a description of the desired circuit into a CAD system. The photograph of FPGA core board and constructed circuit board is shown in figure 5. The captured print screen of the VHDL program in Quartus Prime software is shown in figure 6.

Fig.5 The photograph of FPGA core board and constructed circuit board.

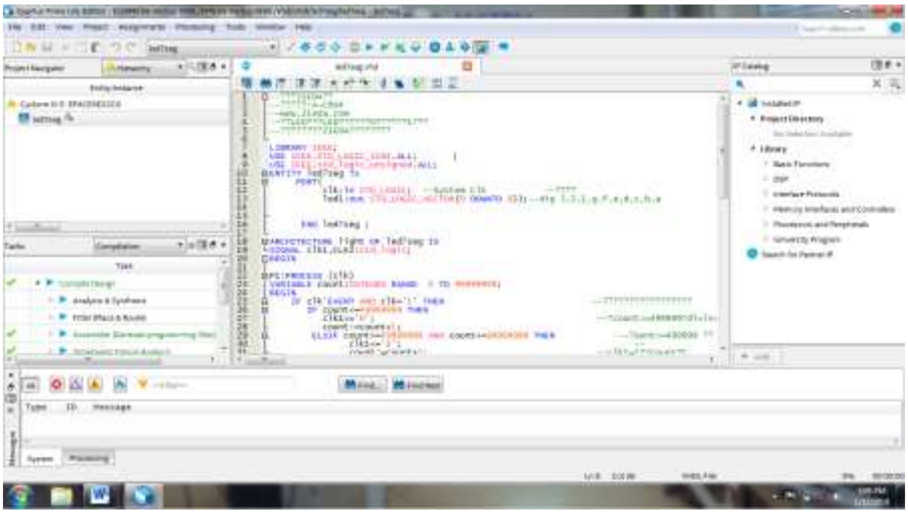
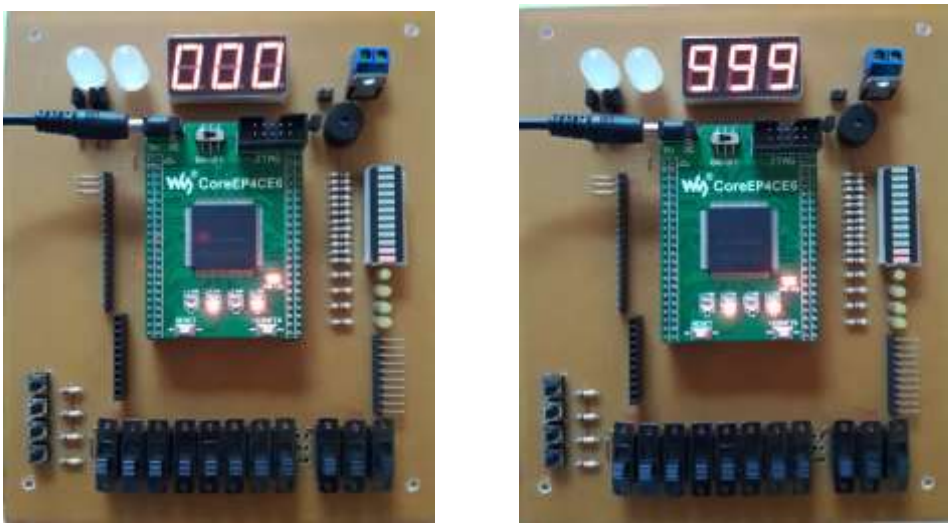


Fig. 6 The captured print screen of the VHDL program in Quartus Prime Software.

Results and Discussion

The design and construction of FPGA-based 3-digit 7-segments LED display counter board had been done successfully. The input and output devices of constructed training board are tested by downloading bit stream files created using VHDL. The programs written in VHDL are also simulated on the computer before loading in the FPGA board by using ModelSim simulator software. The switches and LEDs can be used to do combinational logic circuit and arithmetic circuit experiments. The 7-segment display can be used to study sequential circuits.

The constructed FPGA-based 3-digit 7-segments LED display counter board is reprogrammable unlike fixed logic ICs which are usually used in other counter circuits. Therefore many digital counter functions such as up counting, down counting, event counter, stopwatch counter functions can be implement without requiring to change the constructed circuit board. Valuable programming practices can also be achieved by using this circuit board in Electronics experiments. The constructed board can count numbers “000” up to “999”. The photographs of the constructed FPGA-based counter board doing digital counting are shown in figure 7(a) and figure 7(b), respectively.



(a) (b)

Fig. 7 The photographs of the constructed FPGA-based 3-digit 7-segments LED display counter (a) counting “000” and (b) counting “999”.

Conclusion

The constructed FPGA – based 3-digit 7-segment LED display counter has many input and output circuits together with 7-segments LED display circuit. Therefore the application can be extended to design more complex digital counting circuits by using existing input/output devices as well as adding more input/output devices. It can even be used to design small and medium microcontrollers and microprocessors with wider data buses than conventional microcontrollers.

Acknowledgements

I would like to express special thanks to Dr Maung Maung Naing, Rector, Yadanabon University for his kind permission to carry out this research work. I am grateful to Professor Dr Yi Yi Myint, Head of Department and Professor Dr May Thida Win, Department of Physics, Yadanabon University for their helpful advice and continuous encouragement. I also wish to express sincere appreciation to all teaching staff from the Department of Physics, Yadanabon University and those who helped me in doing the research.

References

W. Klietz, “Digital Electronics A Practical Approach with VHDL” 9^{th} Revised Edition, Pearson, (2012).

Waveshare, “OpenEP4CE6-C User Manual”, (2015). https://www.waveshare.com

Altera Corporation, “Cyclone IV Device Handbook”, (2014)

W. Kafig, “VHDL 101: Everything you need to know to get started” Elsevier, (2011).

P. Horowitz and W. Hill, “The art of electronics”, Low price edition, Cambridge University Press, India, (1989).

T.L. Floyd," Electronic Devices", 7^{th} ed., Prentice-Hall International Inc, New Jersey, (2007).